Architectural Consequences of Radiation Performance in a Flash NAND Device

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***Abstract*—Single-event effects and total ionizing-dose testing was performed on a flash NAND device. The results are presented here and the consequences for error correction architectures are analyzed taking into account the fact that beginning-of-life flash devices are susceptible to data corruption with no external stress applied. The analysis indicates that many typical error correction architectures may be ineffectual because of the variety of radiation effects.**

***Index Terms*— *Index Terms*—SEU, single event upset, heavy ion, error detect and correct, heavy-ion testing, total ionizing dose**

I. Introduction

THE increasing demand for higher memory densities in space electronics has generated significant interest in the use of flash NAND devices on orbit [1]. However, there are a number of features of NAND flash memories that require additional care when they are used in on orbit applications. In addition to being susceptible to single-event effects (SEE) [2]-[5] and total ionizing dose (TID) degradation [6], most NAND devices are subject to corrupted data naturally arising during normal operation conditions. Because of this, NAND devices require error correction code (ECC) schemes even in terrestrial environments [7]-[8], without the degradation seen on orbit due to radiation effects.

In this paper we report TID and SEE results for the flash NAND die used in the DDC 256 Gb (16-bit bus) and 192 Gb (24-bit bus) parts. Using the results of these tests we perform a number of comparisons on the effectiveness of different ECC architectures in reducing the upset rate for this device.

II. Test Procedure

A. Single Event Effects

The devices under test (DUT) were flash NAND memories assembled at DDC in San Diego. Following assembly all parts were functionally tested and operating current was recorded to ensure nominal operating conditions in the beam. Testing was performed at the Texas A&M Cyclotron Institute, Radiation Effects Facility. Various ion beams provide for a wide range of linear energy transfer (LET). The 15 MeV / nucleon beams were used for this test. All tests were performed with the beam at normal incidence and room temperature. The target exposure was typically set for a total accumulated fluence 1E7 ions/cm^2, however the beam would be manually stopped in the event any anomalies were observed.

The SEE test software allows for interface with DUTs mounted on the test board by means of daughter cards. BNC connectors on the test board enable the use of an oscilloscope to detect current transients and allow the software to record beam start and stop. All tests were run at room temp and utilize an "address as data" pattern where unique 32 bit values are stored every 32 bits.

The device was tested in three different modes. In the static test, the device was programmed prior to irradiation, and the pattern was verified immediately prior to irradiation. The DUT was powered on but no reads or writes were performed during irradiation. The DUT was irradiated to a fluence of 1E7 ion/cm^2 and monitored for single event latchup (SEL) or single event functional interrupt (SEFI). Following irradiation, the device was read again, and a final erase-write-verify (EWV) performed to verify functionality.

During read-only testing, the device was programmed prior to irradiation, and the pattern was verified immediately prior to irradiation. The DUT was powered on and read continually during the test. The log file recorded the number of blocks that were read during the test. During irradiation the device was monitored to verify functionality. Following a SEFI the beam was stopped, the current was recorded and an attempt was made to recover the device, first through software intervention, and eventually by cycling device power. Following irradiation, the device was read again, and a final EWV was performed to verify functionality.

For EWV testing, the DUT was powered on and a pattern was continually erased, written, and verified to each block in the device. The log file recorded the number of blocks that were accessed during the test. During irradiation the device was monitored to determine if a SEFI had occurred, and recovery was attempted following beam termination.

B. Total Dose

For the total dose tests, NAND die were attached to small PCBs in order to facilitate connections to the devices tested. Radiation Assured Devices (RAD) ^{60}Co room irradiator was used as the radiation source. Electrical Testing was performed at DDC. The parts were tested under four different operation conditions.

1. Read-only, unbiased during irradiation
2. Read-only, biased during irradiation

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3. Read-write, unbiased during irradiation
4. Read-write, biased during irradiation

Parts tested under read-only conditions were programmed once, prior to initial radiation. At all subsequent irradiation intervals the pattern was verified and read-parameters were measured. For read-write parts, the devices underwent pattern verification prior to re-writing the pattern at each irradiation interval. For all tests, the devices were programmed at 3.6 V immediately prior to irradiation and biased devices were held at 3.3 V during irradiation. All steps were performed at room temperature. Five devices were tested at each of the test conditions. 2 control samples were used, one for the read-write conditions, and one for the read-only conditions. We note that these are die-level tests. The packaged device meets higher TID levels due to radiation shielding incorporated into the package. The effectiveness of DDC's RAD-PAK® package is dependent on the mission radiation environment.

III. Results

A. *Single Event Effects*

Testing the device in static mode with LET=53 MeV cm^2/mg to a fluence of 1E7 indicated no SEL. In two other parts tested at room temperature in EWV mode (LET = 53 MeV cm^2/mg, cross section = 1.5E-7 cm^2) and the other in read mode (LET=87 MeV cm^2/mg; cross section = 5E-6 cm^2) a current increase of about 90 mA was seen. The difference between the static and non-static results suggests that the device is SEL immune and the current increase was the result of bus contention in the device [3].

During the course of irradiation a number of devices failed to respond to software commands, we categorize these devices has being subject to a SEFI. To measure the SEFI cross sections, the beam was manually stopped when an event was observed, and the cross-section was calculated as the inverse of the recorded fluence.

TABLE I
TABULATED DATA FROM THE 32GB NAND FLASH SEE TEST

	LET-No SEFI (MeV cm2/mg)	LET 1st SEFI (MeV cm2/mg)
Read Mode	2.7	8.2
EWV Mode	28.8	33

In read mode at room temperature, the first SEFI was measured at LET=8.2 MeV cm^2/mg. We note that in in the two tests, a total of 5 runs were completed in read mode over the LET range of 8.2 to 8.6 MeV cm^2/mg, only one of these runs recorded a SEFI. The total fluence for all runs was 5.22E7 ions/cm^2. Thus the SEFI cross section at this LET is about 1.8E-8 cm^2/device. The next data point where no SEFI were recorded was at 2.8 MeV cm^2/mg. In EWV mode at room temperature, the first SEFI was recorded at LET=33 MeV cm^2/mg. No SEFI was recorded during irradiation with an LET of 28.8 MeV cm^2/mg. The results are summarized in Table I.

Fig. 1 shows the cross section for single-event upsets as a function of LET. The data was collected by irradiating the devices in read-only or static mode. A final, post beam read was performed on the devices and all bits corrupted were considered to be an SEU. The data recorded here is in good agreement with the values seen elsewhere in the literature [4]-[5].

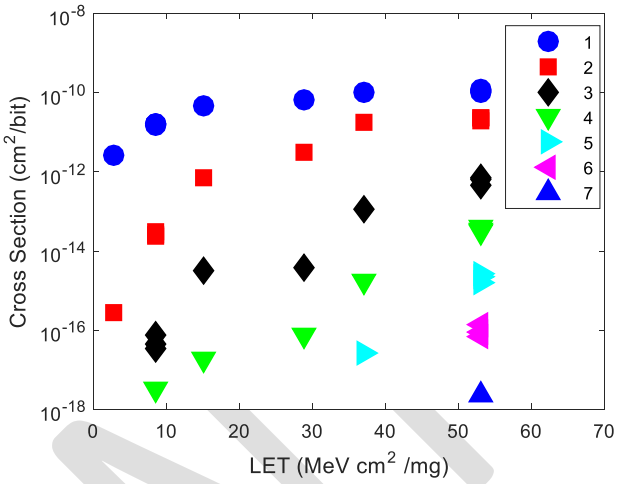

Figure 1 SBU and MBU cross-section. Legend indicates the number of bits corrupted per byte. Data was collected following read mode irradiation.

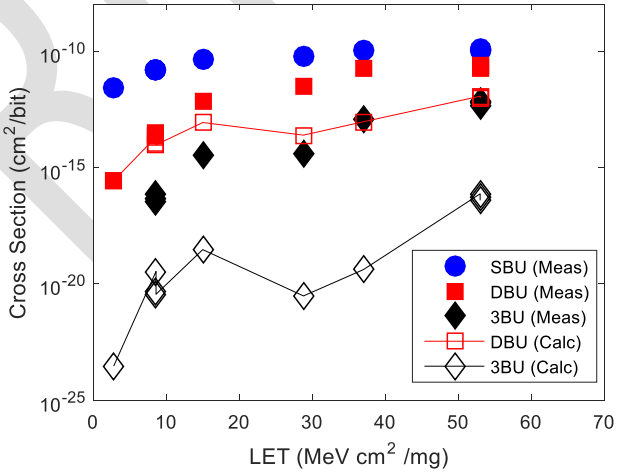

Figure 2 Cross sections for SBU, DBU, and 3BU. Calculations from [9] are shown for comparison

The fluences used in data collection for this test make it possible that the multi-bit errors (MBU) observed were the result of an accumulation of single bit errors (SBU) within a single word. In order to differentiate the MBU contribution from the effects of multiple SBU we used the method of [9] to determine the expected number of accumulated SBU within a single 8 bit word. The results are shown in Fig. 2 where we plot the cross sections for SBU, double bit upsets (DBU) and 3-bit upset (3BU). The lines represent the calculated value for accumulated SBU. The data show that for low LET, most DBU are the result of accumulating SBU. However at higher LET, DBU become more probable, and the DBU cross section is greater than the cross section for accumulated SBU. In contrast, the cross section for 3BU is orders of magnitude higher than the expected cross section for accumulated SBUs. Thus we would expect that the MBU cross sections for 3 (or more) bits are the result of a single ion corrupting multiple data bits.

B. *Total Dose*

All devices passed tests up to a TID level of 41.6 krad. For read-only parts, at the 47.8 krad level, several different failure modes were recorded during pattern verification. In one device, the tester was unable to read the unique ID encoded on the device, in the other parts, the failure was due to an excessive number of bad blocks. The TID test was terminated at this point.

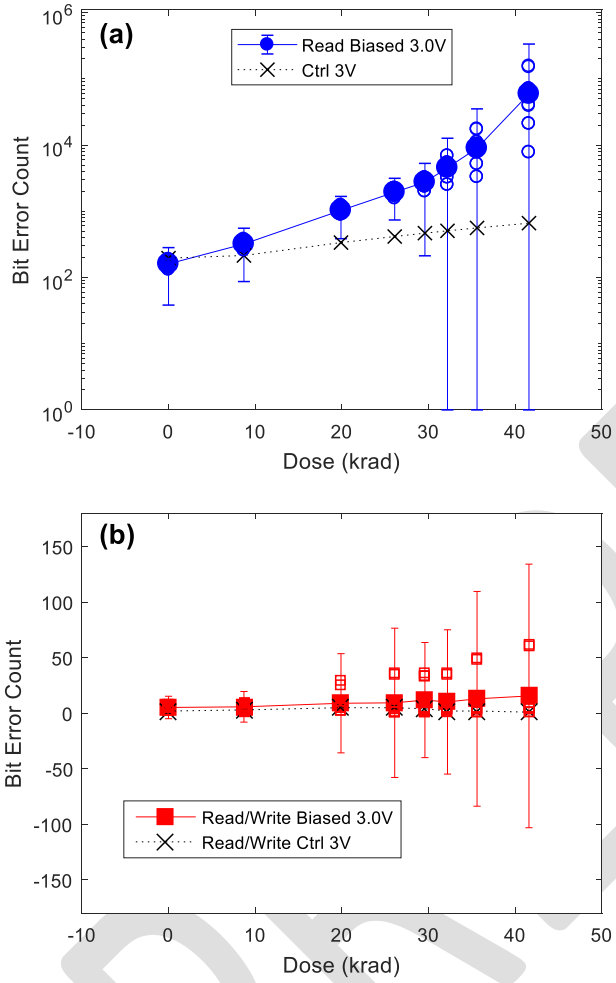

Figure 3 TID data from the (a) read only and (b) read write tests. Biased parts at minimum voltage are shown, max voltage and unbiased parts had nearly identical results. Open symbols represent individual parts. Error bars represent 99% probability, 90% confidence limits.

Following irradiation to 19.9 krad, several read-write parts showed an increased number of bad blocks. It is important to note that for all parts tested there were never more than 8 bad blocks in any part. The specification for device failure was 80 bad blocks. Thus in the discussion that follows we are not dealing with device failures, but the degradation of a small subset of the blocks in the part.

Up to and including the 41.6 krad interval for the read-write parts bad blocks failed because they exceeded the allotted programming time when tested at VCC = 3 V (minimum bias). In Fig. 3 the data for the biased read-write parts are plotted as a function of dose. However both the biased and unbiased parts showed similar degradation regardless of the test conditions.

We note number of bad bits is dependent on the frequency of writes to the part. This test took place over the course of 3 months. For the read write parts, the data was refreshed on an interval between 1 week and 3 weeks long. In fact, the number of errors increased more rapidly for the un-irradiated, read-only control sample than for the irradiated read-write devices (Table 2). Previous studies [10] - [11] saw a similar trend in NAND flash devices. In those papers the devices that were written to had few or no errors, while the read-only devices showed error accumulation. This leads to the somewhat counterintuitive conclusion that before the end of life, the number of errors seen in a NAND device may be more dependent on the write frequency than on the received TID.

TABLE II
TABULATED DATA FROM THE 32GB NAND FLASH TID TEST

Days	Dose (krad)	Read Only (counts)	Read Write (counts)	Read Only Ctrl (counts)
0.0	0	161	34	188
27.7	8.7	354	36	212
48.6	19.9	1030	45	332
62.6	26.1	1939	46	415
76.7	32	6914	49	509
84.8	35.6	21806	60	562
98.8	41.6	1.51E+05	69	662

C. *Baseline Rates*

In order to evaluate the effectiveness of the different architectures, it is necessary to convert the radiation data into a rate. To do this we calculate the SEU rate using CREME96 in a geosynchronous (GEO) orbit. The results for the different error types and modes are summarized in Table 3.

For the total-dose rate, we take into account the fact that the number of errors increased more rapidly for the un-irradiated read-only control sample than for the irradiated read-write devices, and use a linear fit for the read-only control sample as a worst case estimate of the error rate from TID (Fig. 4). We assume that in on orbit use the flash device will be written to on a schedule similar or more frequent than that used in the read-write TID test (once every 1-3 weeks). As long as the endurance conditions were not exceeded, more frequent writes would result in fewer errors. From the linear fit to the read-only control device we get a rate of 6.3 bits/day, or 1.6E-9 upsets/bit/day.

TABLE III
RADIATION INDUCED UPSET RATES FOR THE 32GB NAND FLASH IN GEO

Upset Type	Upset Rate	Time / Upset
SEU	2.7E-9 SEU/bit/day	1.3E11 yr/(SEU/bit)
2 bit MBU	4.3E-14 MBU/bit/day	6.5E10 yr/(SEU/bit)
3 bit MBU	1.2E-17 MBU/bit/day	2.3E14 yr/(SEU/bit)
7 bit MBU	1.5E-18 MBU/bit/day	1.8E15 yr/(SEU/bit)
SEFI Read	3.9E-6 SEU/die/day	7.0E2 yr/SEFI
SEFI EWV	2.1E-7 SEU/die/day	1.3E4 yr/ SEFI
TID Upset	1.6E-9 upset/bit/day	1.7E6 yr/ upset/bit)

NAND Flash typically have an endurance spec between 5k and 100k cycles. In a 15 year mission this would correspond to between 1 and 11 cycles/day. Given the fact that unless the

endurance limit of the part has been reached, devices tend to be relatively error free when re-written to on a regular basis (Fig. 3) we assume that any additional errors due to endurance and retention limits will be accounted for in the worst case estimates used for TID.

We assume no failures due to bad blocks, and these are handled by standard bad block management systems. For comparison, TID testing of the 32 Gb die indicated there would be about 4.5 bad blocks (0.1%) due to TID over the course of the mission.

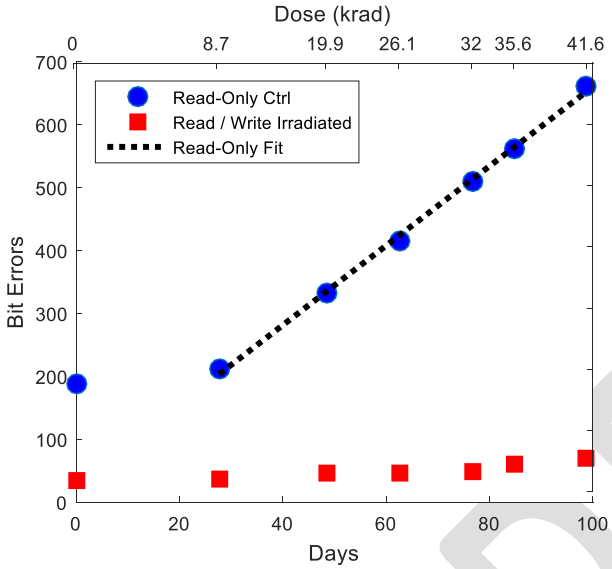

Figure 4 Data for the TID control sample plotted with the data for the irradiated TID read-write devices.

IV. Calculation Methods

A. *Triple Mode Redundancy*

Rates for the failure of triple mode redundant (TMR) devices are based on the method outlined in [12]-[13]. These methods are especially pertinent for the use of the 69F192G24 device which has a 24 bit wide bus to facilitate a triplicated 8-bit wide architecture. The rate of errors that are not corrected by the TMR architecture (R_{TMR}) is given by

$$R_{TMR} = 3MT_c(\mathcal{M}_2 r)^2. \quad (1)$$

For these calculations, the second moment in the text $\mathcal{M}_2$ translates to the number of bits in the triplicated domain. For our case we have bit wise TMR, thus $\mathcal{M}_2$=1, T_c is the time between scrubs, r is the upset rate using the same time units as the scrub rate, and M is the number of groups. This approximation assumes r is small [12].

In talking about single bit level upsets with bit wise TMR, the number of groups would be the number of bits that are triplicated. That is to say with 192 Gb of total memory configured so that there are 64Gb on each leg of the TMR voter as in the 69F192G24, the number of groups M would be 64E9. However in the case of device level SEE such as SEFI, M=2 since there are only 2 groups of 3 die in the TMR configuration (Fig. 5).

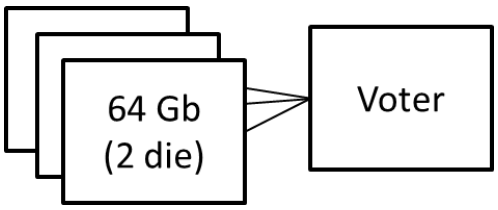

Figure 5 Diagram of TMR configuration.

For the TMR architecture calculations we assume that each leg of the TMR contains 64 Gb (2 die). The voting is performed in a bit wise manner by some external device, and no upsets due to the voter are accounted for in the following calculation. In this configuration, uncorrectable errors (UE) may arise from 2 coincident upsets, 2 SEFIs, or a SEFI in one leg of the TMR with an upset in one of the other (SEFI+upset). Because the voting is bit-wise, any MBU in a single device would be corrected by the voter. We calculate the upset rate for SBU as the sum of the SEU and TID rates from Table 3.

TABLE IV
Upset Rate for System Errors with TMR Correction.

Failure Mode	1 day/scrub UE /device/day	2 weeks/scrub UE /device/day
2 upsets	3.5E-6	5.0E-5
2 SEFI (read)	9.1E-11	1.3E-9
2 SEFI (EWV)	2.6E-13	3.5E-12
SEFI + upset	2.3E-5	2.3E-5

In the case of the SEFI + upset a slightly different method must be used for rate calculation. The methods in [12]-[13] assume identical failure rates for all legs of the TMR memory. We note that when a SEFI occurs any upset will cause a system error. The NAND flash die upset rate in GEO would indicate about 140 upsets/die/day or 1 upset per die every 10 minutes. SEFIs are expected at a much lower rate (Table 3). Thus we would expect that unless the scrub is frequent enough to remove all SEU, system errors occur at the device SEFI rate taking into account that there are six die in the package. The results are summarized in Table 4.

B. *SEC/DED*

The single-error correct, double-error detect (SEC/DED) uses 16 data-bits with 6 check-bits and is capable of correcting a single-bit error in a single address, or detecting a double bit error in the same address location. Error rates ($R_{SEC/DED}$) are governed by the binomial distribution where we are calculating the probability of 2 or more upsets in 22 bits (2 "successes" in 22 tries using the typical description of the binomial distribution). The upset probability is the upset rate multiplied by the time between scrubs.

$$P_{ECC}(m) = R_{ECC}(m) \times T_C = \frac{n!(P)^m q^{n-m}}{m!(n-m)!} \quad (2)$$

Where n is the number of susceptible bits (here n=22); m is the number of upsets ($m \geq 2$) that would cause an uncorrectable

error; P is the probability of a single bit upset; q = 1-P. The results are summarized in Table 5.

We note that a method to calculate the system upset-rate in the presence of ECC codes is derived in [14] to calculate the EDAC word error rate when using single-bit correct double-bit detect ECC. While their methods will work with the SEC-DED system described here, the method must be adjusted to accommodate the BCH architecture discussed in the next section. However following the convention of [14] we calculate the probability of a single bit upset as $P= R_{BF}T_c$ (where R_{BF} is the single bit upset rate). Similarly, we calculate the rate of SEC-DED failures in a single word as:

$$R_{SEC/DED}(m) = \frac{1}{T_C}\sum_{m=2}^{n} P_{SEC-DED}(m). \qquad (3)$$

$P_{SEC-DED}$ falls off rapidly as m increases, and in many practical applications, only the *m*=2 term matters.

For a 64 Gb device (2 die), there would be about 2.9E9 SEC-DED words thus with a 1 day scrub, we would expect the upset rate due to multiple SBU to be about 1.2E-5 UE/device/day. This is higher than the SEFI rate but lower than the rate for DBU. Thus the UE rate cannot be improved with more frequent scrubbing since the MBU rate would be unchanged by the scrub frequency. Error rate improvement beyond the MBU rate would require more robust error correction architecture.

TABLE V
BINOMIAL DISTRIBUTION PARAMETERS AND UE RATE FOR ECC METHODS WITH 1 SCRUB / DAY.

	SEC-DED	BCH
n	22	4320
m	2	9
Multi– SBU 1 scrub/day (UE/dev/day)	1.2E-5	1.1E-41
MBU (UE/dev/day)	2.8E-3	9.6E-8
SEFI /dev/day	7.8E-6	7.8E-6

C. BCH

The BCH uses 512 data bytes and 28 check bytes and is capable of correcting 8 bits in 540 bytes. The BCH upset rate (R_{BCH}) is calculated using Eq. 2 assuming 9 or more "successes" in 540x8=4320 trials (Table 5). For a 64 Gb device, there would be about 1.5E7 BCH words thus with one scrub every day, we would expect the device upset rate to be about 1.1E-41 uncorrected errors/device/day. No 8-bit or higher MBU were recorded during SEU testing, however using the 7-bit MBU cross section as an estimate we would expect a worst case UE rate of 9.6E-8 UE/device/day due to MBU. This is significantly lower than the SEFI rate. Thus we would expect the SEFI rate to determine the system error rate.

D. TMR + ECC

It is also possible to use multiple layers of correction. In Fig. 6-7 we show two architectures that include TMR and ECC codes. In Fig. 6, the TMR die are voted prior to ECC. In Fig. 7, each die is separately subjected to ECC prior to TMR voting. In both cases, a system error will occur when there is a SEFI in two legs of the TMR and we would expect an upset rate of about 9.0E-11 upsets/device/ day with a 1 day scrub (Table 4). However these architectures would be less vulnerable to SEFI+SEU failures that dominate the TMR only architecture. We note that the UE rate in the SEFI + SEU case for both architectures is the product of the SEFI rate and the rate for the appropriate type of SEU.

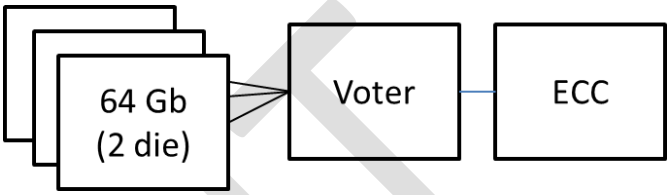

Figure 6 TMR+ECC (TMR first) Architecture – 2 banks of triplicated die, voted bitwise then corrected by ECC

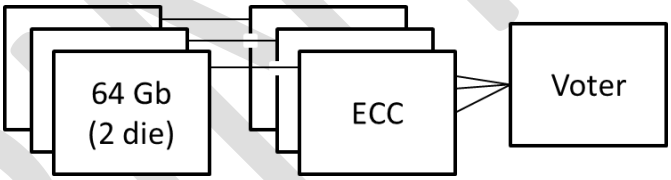

Figure 7 ECC+TMR (ECC-first) Architecture – 2 banks of triplicated die, corrected by ECC then voted.

There is a subtle difference between the performance of the TMR-first architecture (Fig. 6) and the ECC-first architecture (Fig. 7). In the ECC-first architecture the data from each word will be corrected and then voted. Thus a UE will occur when there is a SEFI and the ECC is defeated in one of the other die (Table 6). In this case the UE upset rate will be the product of the SEFI rate and twice ECC rate.

In contrast, for the TMR-first architecture because one die is in SEFI the data from that leg of the TMR is incorrect and the SEU from both of the two operating die will be transmitted by the voter to be corrected by the ECC. Because the TMR votes two words down to one, the ECC is now correcting for m successes in 2n bits (Eq. 2). The size of the target has doubled.

The results are summarized in Table 6. For the BCH architecture, with 1 scrub / day, the UE rate will be dominated by the rate for 2 SEFIs. In contrast for the SEC-DED architecture analyzed here, the UE rate will be dominated by the SEFI +MBU rate.

TABLE VI
UE UPSET RATE FOR TMR + ECC CORRECTION. CORRECTION METHODS CORRESPOND TO FIG. 4-5. RATES ARE FOR 1 SCRUB / DAY

Architecture	Rate SEFI+SEU UE/Device/Day	Rate SEFI+MBU UE/Device/Day
SEC-DED + TMR	2.9E-10	6.4E-8
TMR + SEC-DED	5.9E-10	6.4E-8
BCH + TMR	2.5E-48	2.3E-12
TMR + BCH	1.0E-44	2.3E-12

V. CONCLUSION

Flash NAND devices are subject to data corruption even under terrestrial conditions. The data indicates that the error correction methods used in terrestrial application can be used

to attain relatively low error rates even in the harsh environment of space. Determining NAND UE rate in space requires careful attention to the interplay of the baseline upset-rates for multiple effects as well as architectural considerations such as ECC precedence and scrubbing rates. Because there are multiple different SEE that need to be accounted for care must be taken to ensure that a specific error correction architecture is robust to all possible failure modes. As an example the BCH ECC is robust in correcting bit errors, however it can be defeated by a single SEFI, and as a result, the UE for the system is limited by the SEFI rate. Thus SEFIs must be considered in any NAND architecture for space.

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