Radiation Testing of a Flash NAND Device

D.L. Hansen, F. Meraz, J. Montoya, S. Roberg, G. Williamson

Abstract— **Total ionizing dose and single event effects testing was performed on 4 Gb NAND flash die used in DDC's 69F24G24 flash NAND devices. If the data is regularly refreshed, the devices show good resistance to corrupted bits during total dose irradiation. In the case of heavy ion irradiation, multi-bit upsets could prove problematic to some error correction schemes.**

***Index Terms— Index Terms*—SEU, single event upset, heavy ion, heavy-ion testing, total ionizing dose**

I. Introduction

In addition to being susceptible to single-event effects (SEE) [1]-[4] and total ionizing dose (TID) degradation [5], most NAND devices are subject to corrupted data naturally arising during normal operation conditions. Because of this, NAND devices require error correction code (ECC) schemes even in terrestrial environments [6]-[7], without the degradation seen on orbit due to radiation effects.

In this paper we report total ionizing dose (TID) and single event effects (SEE) results for the 4Gb flash NAND die used in the DDC 24 Gb (24-bit bus) parts. The upset data was analyzed to determine if multiple-bit upsets within a single word were the result of a single ion corrupting multiple bits, or if they resulted from multiple, single-bit upsets accumulating as a result of the high fluences used in testing. For the TID test the increase in bit errors was analyzed to determine changes to the threshold distribution due to cell degradation induced by TID.

II. TID Testing

TID testing was performed at Radiation Assured Devices (RAD) ^{60}Co room irradiator. We note that the tests were performed at a dose rate of 10 mrad/s, thus parts were irradiated for about 1 month to achieve the 21 krad intervals. Electrical Testing was performed at DDC. The parts were tested at minimum and maximum voltage under four different operation conditions.

1. Read-only, unbiased during irradiation,
2. Read-only, biased during irradiation,
3. Read-write, unbiased during irradiation,
4. Read-write, biased during irradiation,

Parts tested under read-only conditions were programmed once, prior to initial radiation. At all subsequent irradiation intervals the pattern was verified and read-parameters were measured. For read-write parts, the devices underwent pattern verification prior to re-writing the pattern at each irradiation interval. For all tests, the devices were programmed at 3.6 V immediately prior to irradiation and biased devices were held at 3.3 V during irradiation. All steps were performed at room temperature. Five devices were tested at each of the test conditions. 2 control samples were used, one for the read-write conditions, and one for the read-only conditions. We note that these are die-level tests. The packaged device meets higher TID levels due to radiation shielding incorporated into the package.

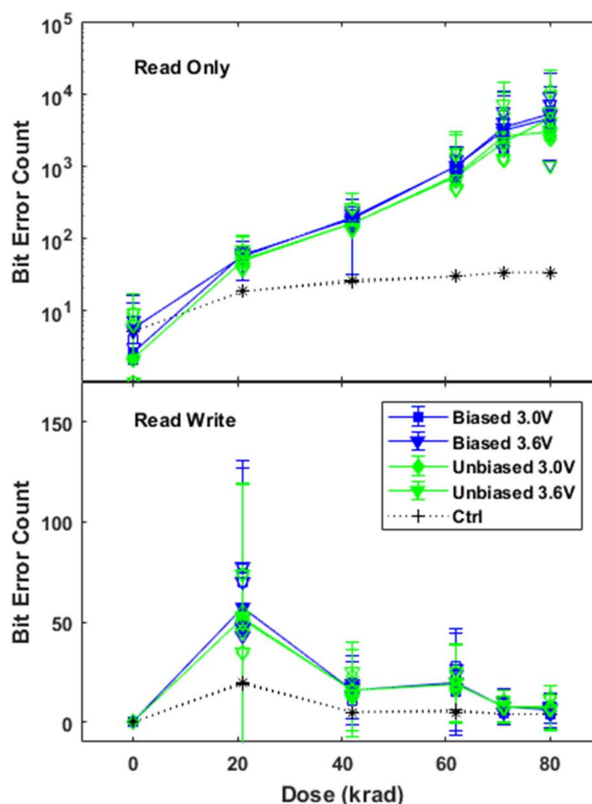

Fig. 1. Average bit error count as a function of dose for the read-only and read-write devices. Error bars are 99% probabilty 90% confidence limits.

For the read-write parts (Fig. 1), the number of bit errors recorded tracked the amount of time between writes. The largest number of errors recorded was at the 21 krad point. This data point corresponds to the time for irradiation plus the time between the initial characterization and irradiation start. For comparison, the 42 krad and 62 krad points had similar numbers of errors, and an identical time between writes. The same can be said for the final two read write points in Fig. 1. The number of errors increased more rapidly for the un-irradiated read-only

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control sample than for the irradiated read-write devices. While the read-only control samples show an approximately linear increase in the number of bit errors, the situation is slightly more complicated for the read-only irradiated devices (Fig. 2). In most cases, the errors seen in the irradiated parts were single bad bits in a block. Previous studies [8-9] have indicated that the distribution of threshold voltages for the NAND storage cells shifts and widens with the increase in total dose. This occurs because the trapped charge increases with irradiation, causing increased cell leakage through trap assisted tunneling and charge de-trapping.

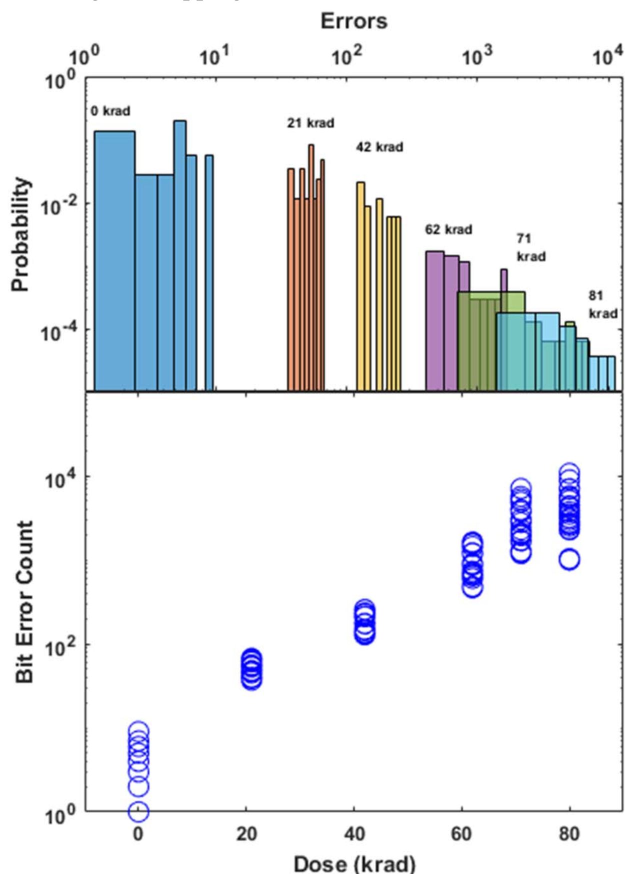

Fig. 2. Bit error count vs. dose plotted for all read-only devices tested. The top of the plot gives the histogram for all parts at a specific dose. Note axes are logarithmic.

TABLE I
DISTRIBUTION PARAMETERS FOR BIT ERRORS IN READ ONLY DEVICES

Dose	Mean	Standard Deviation
0	3.1	3.0
21	53	9.6
42	172	44.5
62	859	397
71	2765	1748
81	4311	2532

To look at this further, in Fig. 2 we plot the total bit errors for each part tested as a function of dose, and then plotted a histogram of all parts at each dose point (Fig. 2, top). The histogram was fit with a normal distribution and the results are recorded in Table I to quantify the increase and the spread in the distribution of bit errors for the parts tested. The parameters in Table I represent a distribution fit to all parts.

During TID irradiation, all parameters remained within specification up through the 42 krad data point. The standby current exceeded specification for one biased part at the 62 krad level (Fig. 3), while the standby current for the unbiased parts remained in specification through the terminal dose level of 80 krad. In comparison the VCC Active Read array current (Fig. 4) remained in specification and the parts remained functional throughout the test.

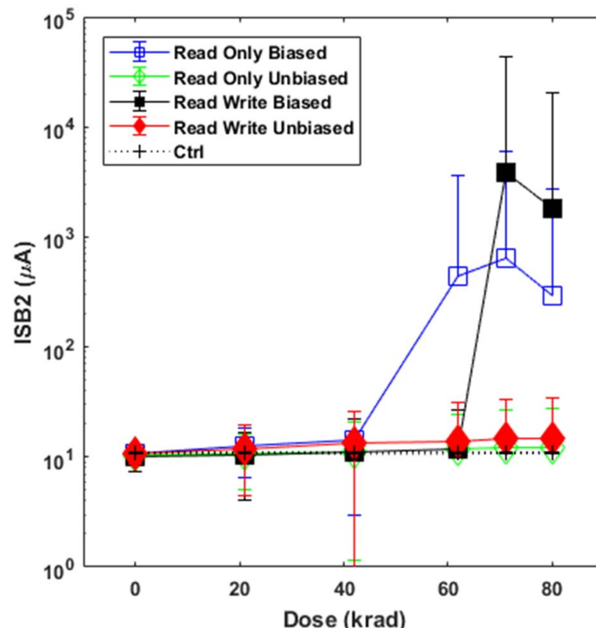

Fig. 3. Standby leakage current vs. dose plotted at minimum (3.0 V) bias. Biased parts are worst case. Note axes are logarithmic, and error bars represent 99% probability, 90% confidence levels.

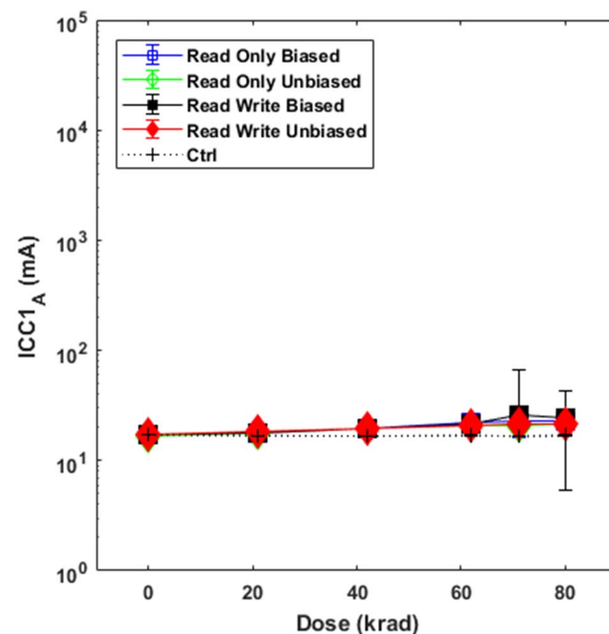

Fig. 4. VCC Active Read array current vs. dose plotted at minimum (3.0 V) bias. Error bars represent 99% probability, 90% confidence levels.

III. SEE Testing

Testing was performed at the Texas A&M Cyclotron Institute Radiation Effects Facility. Various ion beams provided a wide range of LET. The 15 MeV / nucleon beams were used for this test. The SEE tester software ran on a laptop with PCI Express as the interface to the test board. This allowed the configuration to be programmable and interface to a variety of DUTs mounted on the test board by means of daughter cards. BNC connectors on the test board enabled the use of an oscilloscope to detect current transients and allowed the software to record when the beam was on. All tests were run at room temp and utilized an "address as data" pattern where unique 32 bit values were stored every 32 bits. The device was tested in three different modes.

In the static test, the device was programmed and the pattern verified immediately prior to irradiation. The DUT was powered on statically in the beam. That is no reads or writes were performed. The DUT was irradiated to a fluence of $1{\times}10^7$ ion/cm^2 and monitored for SEL. Following irradiation, the device was read again, and a final EWV performed to verify functionality.

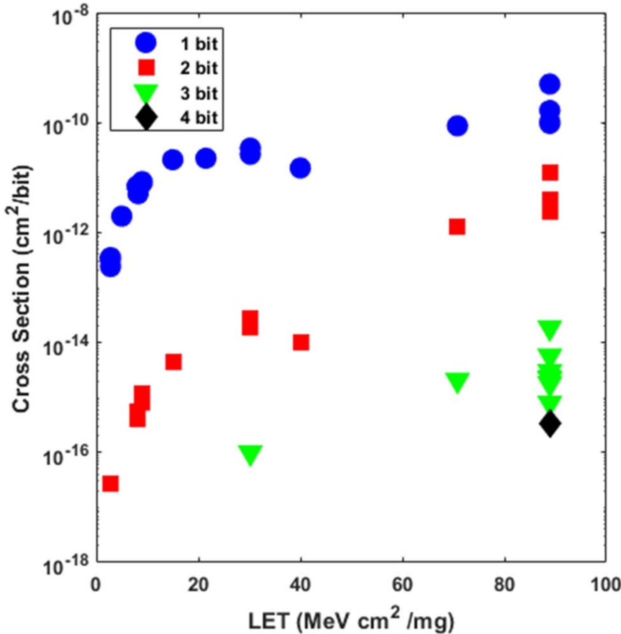

Fig. 5 Number of bits corrupted per byte. Data was collected following read mode irradiation.

During read-only testing, the device was programmed, and the pattern verified immediately prior to irradiation. The DUT was powered on and a log file recorded the number of blocks that were read during the test. During irradiation the device was monitored to determine if a SEL / SEFI had occurred, at which point the beam was stopped. The current was recorded and an attempt was made to recover the device, first through software intervention, and eventually by cycling device power. Following irradiation, the device was read again, and a final EWV was performed to verify functionality.

For erase-write-verify (EWV) testing, the DUT was powered on and a pattern was continually erased, written, and verified in each block in the device. The log file recorded the number of blocks that were accessed during the test. During irradiation the device was monitored to determine if a SEL / SEFI had occurred. Following a SEL /SEFI the beam was stopped. The current was recorded and an attempt was made to recover the device to recover the device; first through software intervention, and eventually by cycling device power. Following irradiation, a final EWV was performed to verify functionality.

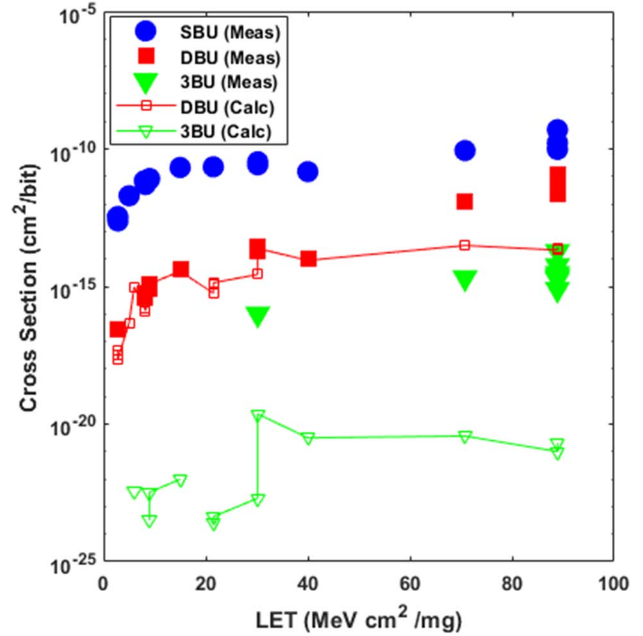

Fig. 6 Number of bits corrupted per byte following read only mode irradiation (solid symbols) and the calculated cross section for MBU resulting from accumulated SBU (open symbols). Measured data is the same as in Fig. 5.

The cross section for number of bits corrupted in a byte is plotted in Fig. 5. Single bit upsets (SBU) are the most common, with the cross section for SBU being 2-3 orders of magnitude greater than the cross section for double bit upsets (DBU) at low LET. To analyze the multi bit upset (MBU) cross sections further, in Fig. 6 we plot the same data as in Fig. 5 but only include the cross section for SBU, DBU, and 3 bit/byte upsets (3BU). In addition, using the method found in [10] we calculate the expected cross sections for DBU and 3BU assuming that all multi-bit errors are the result of an accumulation of SBU, rather than resulting from a single ion corrupting multiple bits. This method uses the expression

$$f(2) = \frac{4k(k-1)}{M \times N} \qquad \text{Eq. 1}$$

to determine the number of "false" DBU created by the accumulation of single bit upsets within a word. Here, $f(2)$ is the number of false DBUs, k is the total number of upsets, M is the number of words, and N is the number of bits per word. The expression can be applied sequentially using the calculated value for $f(2)$ to find $f(3)$, the number of words with 3 bits corrupted because of an accumulation of SBUs:

$$f(3) = \frac{4 \times f(2)[f(2)-1]}{M \times N} \quad . \qquad \text{Eq. 2}$$

In comparing the measured and calculated data, we note that there is fairly good agreement between the calculated an measured values for DBU at low LET indicating that in this LET range, the 2-bit upsets are result of an accumulation of SBU. The tests are only sensitive to events with a cross section greater than 2.5×10^{-17} cm^2/bit (1 upset, with 1×10^7 ion/cm^2 fluence). The calculated cross section for 3BU is well below that limit, and thus it is not surprising that no 3-bit upsets are seen at low LET. At LET>30 MeV cm2/mg, more 3BU were measured than would be expected based on the calculated values. This indicates that as the LET gets higher, eventually, enough charge is deposited to corrupt multiple bits with a single ion.

Upsets in the device were predominantly transitions from 0 to 1. The cross section for 0 to 1 transitions was several orders of magnitude higher than the cross section for transitions from 1 to 0 (Fig. 7).

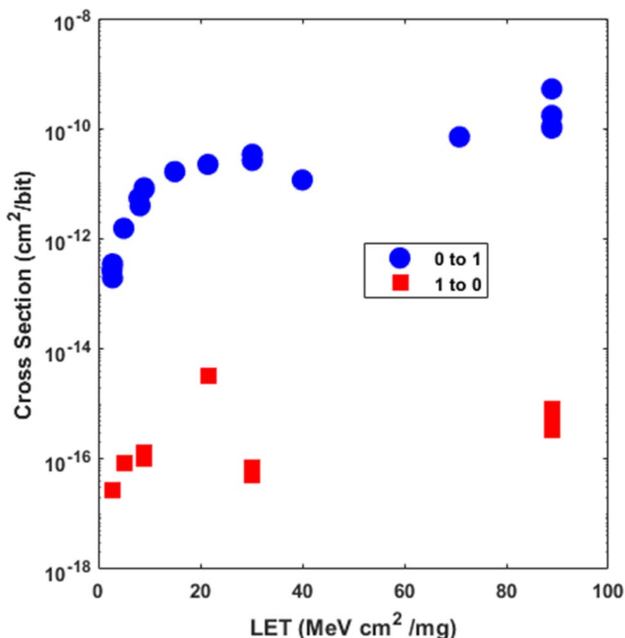

Fig 7 Cross section as a function of LET for SEU causing a transition from a 0 to 1, or 1 to 0. Errors in data bits storing a "0" have a much higher cross section than in cells storing a "1".

IV. Conclusion

TID and SEE data was collected on a 4 Gb flash NAND device. The TID data indicated that the bit error count remains relatively low when the data is refreshed on the time scale of the experiment (about 1/month), and in fact the total number of errors recorded in the devices that were irradiated and refreshed was less than the number of error seen in the un-irradiated control samples used in the read-only tests. In the case of data that was stored and only read, the irradiated devices showed a super-linear increase in the number of errors, and the distribution of errors on the devices had an increasing mean and width. SEE data from the devices indicated that at low LET the devices were unlikely to experience a MBU. This changes at higher LET where the cross section for MBU exceeds the cross section for multiple SBU accumulated within a single word. This has significant implication for ECC architectures, since an MBU corrupting enough bits can, in a single event, defeat an ECC scheme that lacks sufficient robustness.

V. References

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