Radiation Performance of a Flash NOR Device

D.L. Hansen, R. Hillman, F. Meraz, J. Montoya, G. Williamson

Abstract—**We present the results of single-event effects (SEE) and total ionizing-dose (TID) testing performed on the die used in DDC's 56F64008 flash-NOR devices. The device was single event latchup (SEL) immune at LET=85 MeV cm²/mg. All single event functional interrupts (SEFI) observed could be cleared by resetting the part without a need for power cycling.**

Index Terms— **SEU, single event upset, heavy ion, error detect and correct, heavy-ion testing, total ionizing dose**

I. Introduction

THERE has been tremendous interest in flash memory devices in recent years [1]-[9]. Most of this interest has focused on NAND flash devices, which enjoy wide popularity because of their high memory-density. NAND devices require error correction code (ECC) schemes even in terrestrial environments, without the degradation seen on orbit due to radiation effects [10]-[11], In contrast, NOR flash devices tend to offer lower density, but are significantly less vulnerable to single event effects (SEE).

In this paper we report total ionizing-dose (TID) and SEE results for DDC's 56F64008 flash NOR devices. During room temperature testing the device was single event latchup (SEL) immune at LET=85 MeV cm²/mg. All single event functional interrupts (SEFI) observed could be cleared by resetting the part without a need for power cycling. Single event upsets (SEU) consisted of single-bit errors, with a much smaller probability of double-bit errors (DBU) and stuck bits. The die were evaluated for TID tolerance in biased and unbiased conditions in read / write and read-only mode. TID tolerance was dependent on operation mode.

II. TID Testing

TID testing was performed at Radiation Assured Devices (RAD) ^{60}Co room irradiator at a dose rate of 10 mrad/s. Electrical testing was performed at DDC. The devices were tested in 5 groups:

1. Read-only, unbiased during irradiation,
2. Read-only, biased during irradiation,
3. Read-write, unbiased during irradiation,
4. Read-write, biased during irradiation,
5. Design of Experiment (DOE) – read only biased

For all tests, the devices were programmed at 3.0 V, and biased devices were held at 3.3 V during irradiation. The exception to this is the DOE parts described below.

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Parts tested under read-only conditions were programmed once, prior to initial radiation. At all subsequent irradiation intervals the pattern was verified and read-parameters were measured. For read-write parts, the devices underwent pattern verification prior to re-writing the pattern at each irradiation interval. All steps were performed at room temperature with five devices tested at each test condition. Two control samples were used, one for the read / write conditions, and one for the read-only conditions. In addition to the main test groups, an additional two devices were tested using a full factorial DOE. Devices were programmed with a 5555aaaa pattern. Across the sectors of a single die, the voltage was varied from 3.0V to 3.6V in 100mV increments (7 levels), the sector was programed once or 5 times (2 types), and programmed one word at a time or a single page at a time (2 types) for a total of 28 scenarios (Table 1). These devices were only programmed prior to irradiation, similar to the read-only test.

TABLE I
PROGRAMMING MODES FOR THE DOE DEVICES.

Sector	Voltage (V)	Programming Mode	Number of Writes
0	3.0V	word	1x
1	3.0V	word	5x
2	3.0V	page	1x
3	3.0V	page	5x
4	3.1V	word	1x
5	3.1V	word	5x
6	3.1V	page	1x
7	3.1V	page	5x
8	3.2V.	word.	1x.
		Etc.	

NOR devices that were biased and written to during irradiation proved to be the most sensitive. For these devices, the failure mode included the appearance of bit errors at 14.2 krad (Fig. 1). The final dose level passed was 11.4 krad. At 14.2 krad, the corrupted bits were exclusively transitions from "0" to "1". Unbiased read/write devices were subject to the same failure mode (bit errors) as biased devices. However, the unbiased devices did not show bit errors until 27.8 krad (Fig. 1), with a final passing dose level of 25.4 krad.

The read-only tested devices (Fig. 2) showed a higher TID tolerance than the read/write devices. One read-only biased part showed one-bit error starting at 21 krad. The read-only, unbiased devices did not show any failures at the final TID level of 30.7krad. We note that the read-only parts were only tested with a checkerboard pattern.

For the DOE parts, a 1-bit error was recorded at 24 krad. Thus while the different programming modes improved the reliability of the stored data, because data corruption was not the lowest TID level failure mode, the programming methods did not improve the total TID sensitivity of the part.

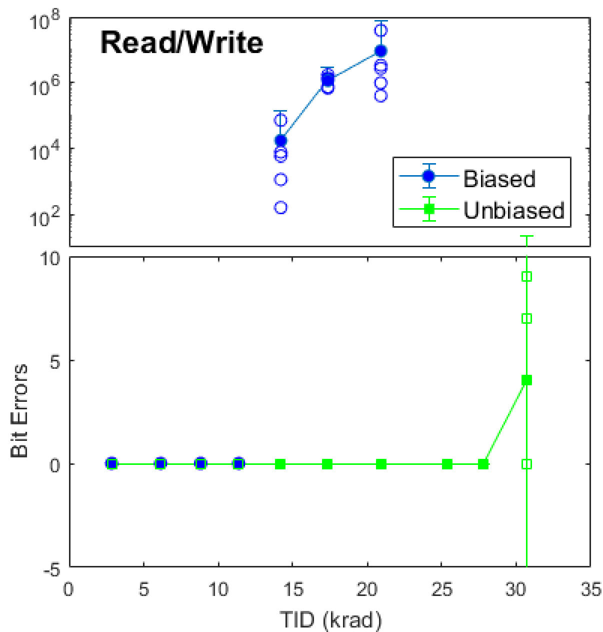

Fig. 1 Bit errors vs. dose for the read/write devices. The y-axis break represents a change in scale. Solid symbols represent the mean, open symbols represent the individual devices, and error bars represent the P99/C90 statistics.

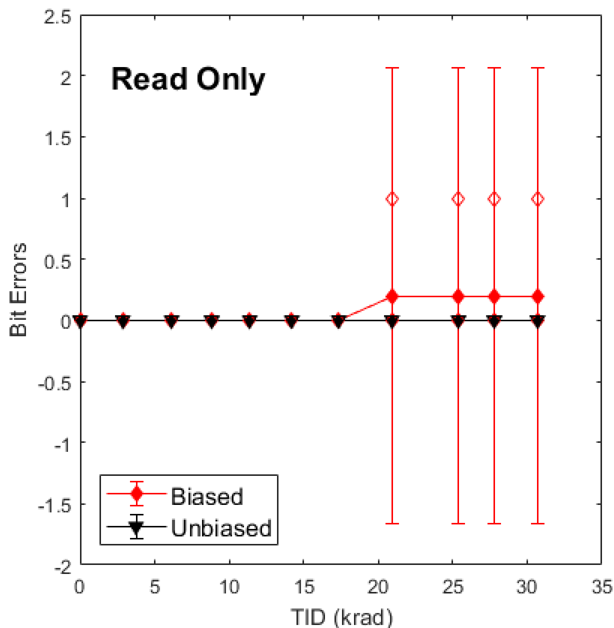

Fig. 2 Bit errors vs. dose for read-only devices. Solid symbols represent the mean, open symbols represent the individual measurements, and error bars represent the P99/C90 statistics.

III. SEE Testing

Testing was performed at the Texas A&M Cyclotron Institute Radiation Effects Facility. Various ion beams provided a wide range of LET. The 15 MeV / nucleon beams were used for this test. The SEE tester software ran on a laptop with PCI Express as the interface to the test board. This allowed the configuration to be programmable and interface to a variety of DUTs mounted on the test board by means of daughter cards. BNC connectors on the test board enabled the use of an oscilloscope to detect current transients and allowed the software to record when the beam was on. All tests were run at room temperature and utilized an "address as data" pattern. The device was tested in three different modes. In the static test, the device was programmed and the pattern verified immediately prior to irradiation. The DUT was powered on statically in the beam. That is no reads or writes were performed. The DUT was irradiated to a fluence of 1E7 ion/cm^2 and monitored for SEL. Following irradiation, the device was read again, and a final EWV performed to verify functionality.

During read-only testing, the device was programmed, and the pattern verified immediately prior to irradiation. The DUT was continually read during irradiation, and a log file recorded the number of blocks and errors that were read during the test. During irradiation, the device was monitored to determine if a SEL / SEFI had occurred, at which point the beam was stopped. Following irradiation, the device was read again, and a final EWV was performed to verify functionality.

For erase-write-verify (EWV) testing, the pattern was continually erased, written, and verified in each block in the device. During irradiation, the device was monitored and the beam was stopped following a SEL /SEFI. Following irradiation, a final EWV verified functionality.

A. SEL

SEL testing was performed in static mode. This allowed the device to reach larger fluences without the beam-run being interrupted by a SEFI. The DUTs were tested at six LETs between 37 MeV cm^2/mg and 85 MeV cm^2/mg and 4 temperatures between room temperature and 125ºC (Fig. 3). The flash NOR was immune to SEL at 37 MeV cm^2/mg. At an LET of 52 MeV cm^2/mg and 60 MeV cm^2/mg the device did not latch up at 85ºC, but was vulnerable at 105ºC. At 85 MeV cm^2/mg, no SEL were observed at room temperature (Table 2).

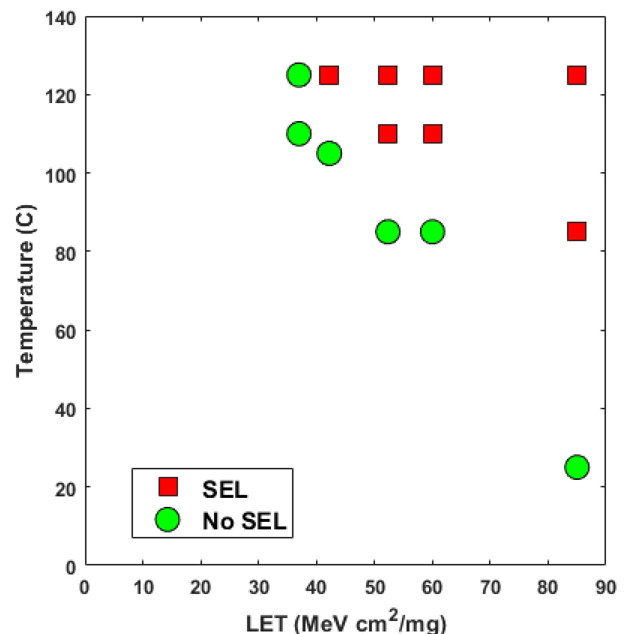

Fig. 3 SEL immunity plotted vs temperature and LET. Green circles indicate no SEL recorded.

The SEL were characterized by increases in the core current between 20mA and 95mA, with the pre-SEL current typically being about 5mA. For the SEL observed, changes in the IO current were less than 0.5mA, thus indicating that the IO was not vulnerable to SEL. The results of the post-irradiation check of the device were not uniform, in some cases the DUT appeared to work normally, while in others, the DUT lost the ability to write or erase.

TABLE II
TEST CONDITIONS FOR SEL IMMUNITY

	25ºC	85ºC	105ºC	125ºC
LET (MeV cm^2/mg)	85	60	42.2	37
DUTs Tested	8	1	3	1
Fluence (cm^{-2})	5E7	1E7	3E7	1E7

B. SEFI

To measure the SEFI cross sections (Fig. 4), the beam was manually stopped when a SEFI was observed, and the cross section was calculated as the inverse of the recorded fluence For EWV mode no SEFI were measured at LET ≤ 42 MeV cm^2/mg; the first was recorded at 51.5 MeV cm^2/mg. In read-only mode, SEFI were recorded at LET = 15.1 MeV cm^2/mg while the highest SEFI-free LET was 8.3 MeV cm^2/mg. A part reset cleared all SEFIs. Power cycling was not required.

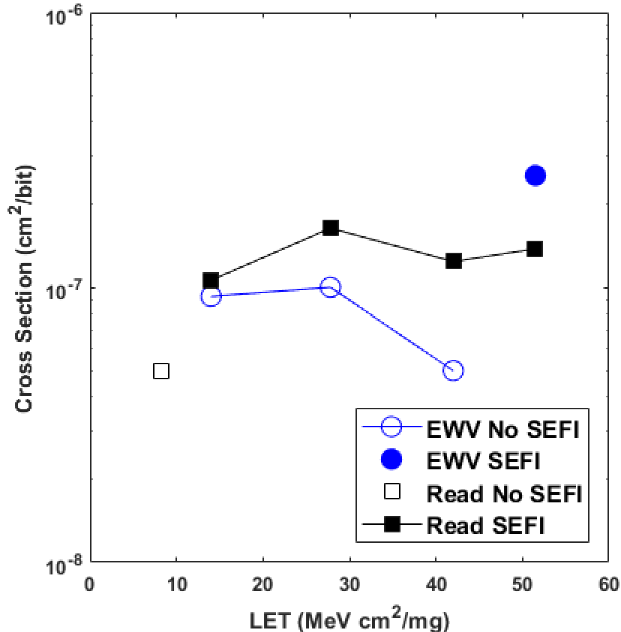

Fig. 4 Cross section as a function of LET for EWV-mode and read-mode SEFI. Open symbols represent the inverse of the fluence for runs with no SEFI recorded. Solid symbols represent the SEFI cross section.

C. Stuck Bits / Bad Blocks

In order to measure the likelihood of stuck bits, all irradiated devices were tested in the lab after they returned from TAMU after the end of the beam run. Upon their return, all devices were read, and then subjected to an EWV cycle. Data that was corrupted after the final post-beam EWV cycle were considered stuck bits.

During read-mode testing two of the 32 devices tested showed stuck bits (Fig. 5). For the data point at 85 MeV cm^2/mg, a single block had 13 single bit errors that remained bad following a post-beam EWV. The data point at 14 MeV cm^2/mg had 47150 SBU and 17 DBU after the post beam EWV. These corrupted bits appeared to be associated with write protect bits that were stuck at zero, thus preventing the bits from being erased. In both cases the device could be read.

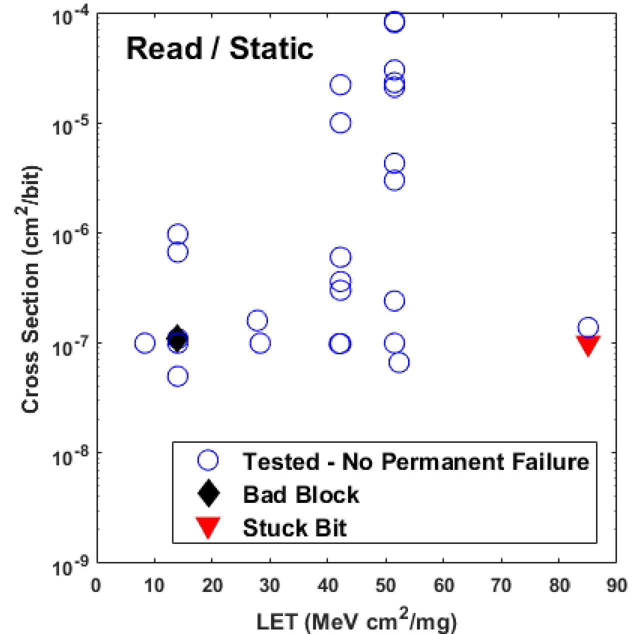

Fig. 5 Cross section for stuck bits following irradiation in read or static mode. Each data point represents a single device. Open symbols represent devices where a post beam run EWV did not show any errors. Solid symbols represent devices with stuck bits.

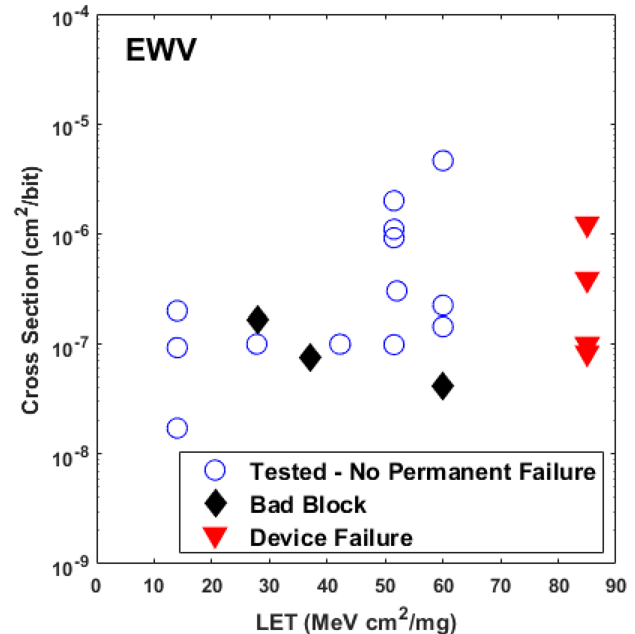

Fig. 6 Cross section for bad blocks following irradiation in EWV mode. Each data point represents a single device. Open symbols represent devices with no bad blocks. Solid diamonds represent devices where half or more of the blocks were bad.

In EWV mode (Fig. 6) we note two failure modes. The "bad block" failure mode was seen in three devices. At LETs of 28 and 37 MeV cm^2/mg 1 or 2 blocks (respectively) showed errors that were not corrected by a post beam run EWV. At an LET of 60 MeV cm^2/mg, 64 blocks were bad. The "bad device" failure mode was only seen at an LET of 85 MeV cm^2/mg. Five devices had half or more of their blocks in error following the post beam run EWV. We note that in (Fig. 5-6) the open symbols represent devices where a post beam run EWV did not show any errors. Thus, the data points plotted are calculated as the inverse of the fluence during a specific run, and represent the upper bound of the cross section.

D. SEU

For SEU testing in read mode the upset data was primarily single bad bits within a byte. During testing, we observed bytes with 2 upset bits with a cross section that was about 2 orders of magnitude smaller than the cross section for single bit upsets. Typically, no bytes were observed with more than 2 bits corrupted during read mode tests (Fig. 7). The exception to this was a single device tested at LET=42 MeV cm^2/mg. For this device, two blocks were corrupted following irradiation in static mode to a fluence of 1E7. The errors were not permanent.

In order to determine if the bytes with two bit-upsets resulted from a single ion causing a double bit upset (DBU), or multiple ions causing an accumulation of single bit upsets (SBU), we followed the procedure outlined in [12]. To describe it briefly, following an upset to any single byte, the probability of the next ion upsetting a second bit in the same byte is $7/b$ since there are 7 additional bits per byte, and b= 512E6, the total number of bits per device. The third ion would then have a probability of $(7\times2)/b$ since there are now at most two bytes in the device where an additional upset will result in two corrupted bits per byte. Generalizing, the probability that the i-th ion hits a position to create a byte with two corrupted bits is

$$p_2 \leq 7(i\text{-}1) / b. \quad (1)$$

For an experiment with k events, if k <<b, we have the total number of bytes that accumulate 2 upset bits is

$$n_2 = \sum_{i=2}^{k} p_2 = \frac{7}{2}\frac{k(k-1)}{b} \quad (2)$$

In Fig. 7, we plot the measured cross-section for SBU, and the measured cross-section for all bytes where there are 2 bits corrupted (accumulated SBU + DBU) along with the calculated (Eq. 2) cross-section for DBU that are the result of accumulated SBU. The similarity of the calculated cross section to the measured cross section indicates that the likelihood of a single ion corrupting multiple bits is very small.

Because of the amount of time to perform a complete EWV on each block during EWV testing, the entire device was not tested before the terminal fluence of 1E7 ions/cm^2 was reached. Thus in the cross section analysis presented here, the data was first normalized to calculate cross section per sector, then that value was converted to the more familiar cross-section per bit.

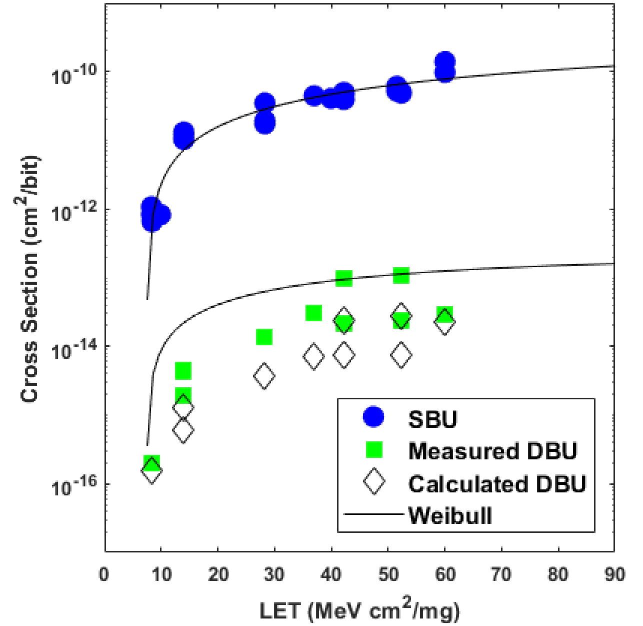

Fig. 7 Cross section for measured SBU, measured DBU, (accumulated SBU +DBU) and the calculated cross section for DBU due to an accumulation of SBU for devices operated in read mode. Solid lines represent Weibull fit

E. Upset Rates and Error Correction

Using the Weibull fits shown in Fig. 7 we calculated the upset rates for SBU and DBU using CREME96 [13] assuming a geosynchronous orbit and 100 mils of shielding. For SBU, we get an upset rate of 2.2E-13 upset/bit/day or 1 upset every 24 years for the device. Thus with a simple SEC-DED error correction the error rate will be determined by the DBU upset rate which we calculate as 1.9E-15 upset/bit/day or 1 upset every 2700 years.

IV. Conclusion

Single event effect (SEE) testing was performed on the 56F6408RP 512Mb NOR flash device in static, read only, and EWV mode. The SEL threshold was temperature dependent, with no SEL recorded at room temperature and LET=85 MeV cm^2/mg. In read mode the first SEFI was recorded at LET=15.1 MeV cm^2/mg with no SEFIs recorded at 8.3 MeV cm^2/mg. In EWV mode the first SEFI was recorded at LET=51.5 MeV cm^2/mg with no SEFIs recorded at 42 MeV cm^2/mg. A reset cleared all SEFIs. Single event upset (SEU) saturated cross-section was about 1.7E-10 cm^2/bit with a threshold of about 10 MeV cm^2/mg. Upsets were typically single corrupted bits with a smaller cross section for DBU and stuck bits.

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